Avoid Instability in Rail to Rail CMOS Amplifiers

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Introduction

The minimum feature size of the MOS transistor has been greatly reduced since its invention just a few decades ago. Reductions in gate oxide thickness, channel length and width have been responsible for a revolutionary reduction in overall circuit size and power consumption. As the gate oxide thickness decreases the maximum allowable power supply voltage decreases; channel length and width reductions provide smaller and faster device performance. These device enhancements have afforded the development of high frequency CMOS rail-to-rail I/O amplifiers in answer to the modern system designers increasing demand for analog circuits capable of operation at the same low supply voltage as their digital counterparts.

This paper addresses the important issues uniquely related to the new generation of CMOS rail-to-rail amplifiers. Beginning with a general discussion and description of classic voltage feedback and current feedback amplifier circuit topologies and the most common causes of feedback amplifier oscillation. Then the CMOS rail-to-rail amplifier circuit is divided into 4 basic blocks for analysis and discussion; input, intermediate gain, output and feedback network stages. The frequency dependent gain and phase shift of each stage will be presented, after which a complete system simulation of all 4 basic circuit blocks will be presented and discussed. The second section of this appnote will present and discuss the mechanism, trade-offs and benefits of 3 practical solutions to the amplifier oscillation issue.

Voltage Feedback Amplifier

Figure 1 shows a simplified schematic of the EL5157, a very popular high bandwidth voltage feedback amplifier. A classic differential input stage drives the folded cascode second stage, which converts the differential voltage of the input stage into a current at the high impedance gain node where it is realized as the high voltage gain of the amplifier.

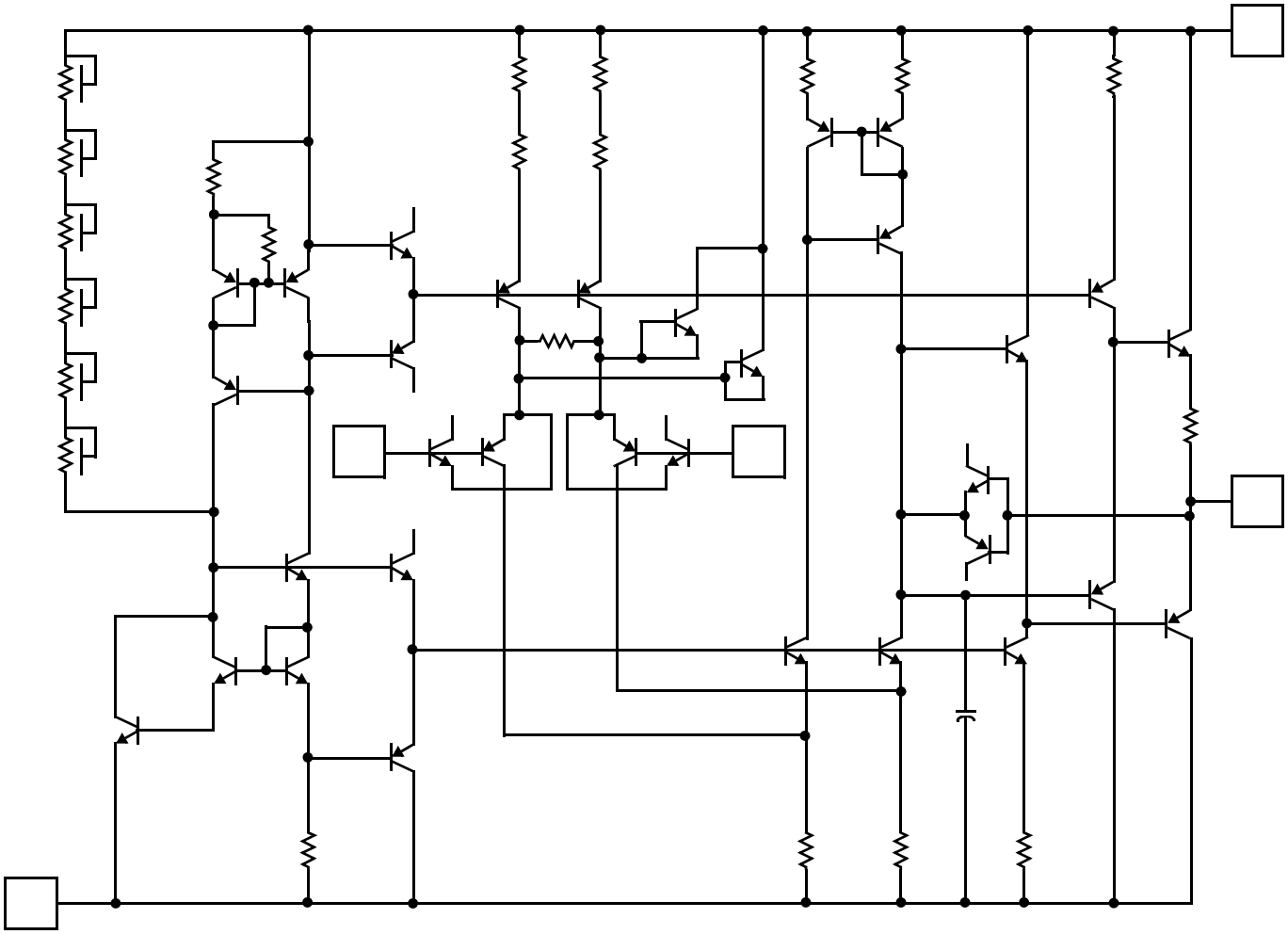


FIGURE 1. VOLTAGE FEEDBACK AMPLIFIER

Essentially, the output impedance of the second stage current source becoming an output signal at the high impedance node multiplies any current difference occurring in the signal-path transistors. The output stage is a push pull class AB buffer and simply buffers the high voltage gain to the single ended output of the amplifier.

Output Inductance

An inductor is an electrical component with frequency dependent impedance characteristics; an inductor exhibits low impedance at low frequencies increasing to higher impedance at higher frequencies. While the "ideal" operational amplifier output impedance characteristic is zero the output impedance of "real" amplifiers is inductive and like the inductor increases with increasing frequency. The output impedance of the EL5157 is shown in Figure 2. A common challenge in applications using operational amplifiers is driving a capacitive load. A challenge because the inductive output of the op amp in conjunction with the capacitive load creates an LC resonant tank topology where the capacitive load reactance in conjunction with the inductive drive impedance results in extra phase lag when feed back is closed around the loop. Decreasing phase margin introduces the possibility of amplifier oscillation. When oscillating, the amplifier becomes very hot and can self-destruct. There are a couple of very well known solutions to this challenge. 1) The simplest solution is the addition of a resistor in series with the output to force the feedback to come from the amplifier's direct output while isolating the reactive load. The trade off of this method is the sacrifice of a small amount of the output voltage swing across the load. 2) Another straightforward solution is the application of a "snubber network". The snubber is a resistor and capacitor placed in parallel with the capacitive load providing resistive impedance across the load to diminish the output phase shift; providing additional stability.

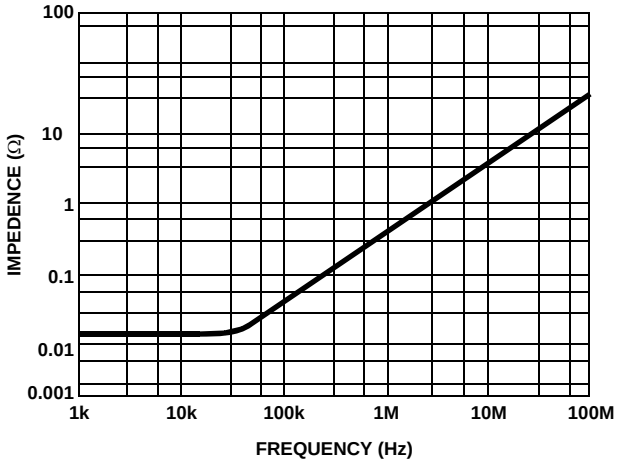


FIGURE 2. EL5157 OUTPUT IMPEDANCE

Current Feedback Amplifier

While current mode feedback operational amplifiers have been around for a long time, their high slew rate, high bandwidth and low distortion is responsible for their current popularity with ADSL systems and HDTV application designers.

Figure 3 shows a simplified drawing of a current mode feedback amplifier (CFA) EL5160. The +input is high impedance and buffered directly to the -input through transistors Q_6 & Q_7 and Q_{10} & Q_{11}. It is this very low impedance of the -input stage that differentiates CFA and voltage mode feedback topologies and provides the CFA with unique advantages. Q_7 and Q_{11} drive the current mirrors in the signal path of the high impedance node at the base of Q_8 and Q_{12}. These current mirrors supply current on demand to the high impedance node from the power supply providing the CFA an extremely high slew rate. The voltage level at this high impedance node is buffered to the output by emitter followers Q_9 and Q_{13}. Feedback connected from the output to the negative input forces the -input current to zero. A feedback resistor or resistor divider connected from output to the negative input converters the error voltage (voltage difference between V_{OUT} and V_{IN-}) into an error current. The amount of feedback is determined by the feedback resistor value. Every current feedback amplifier specifies an optimal feedback resistor value for highest bandwidth while maintaining stable operation. If feedback resistor smaller than the specified resistor is used, oscillation becomes a possibility. The CFA is also called a transimpedance amplifier because any change in the -input current results in change in output voltage.

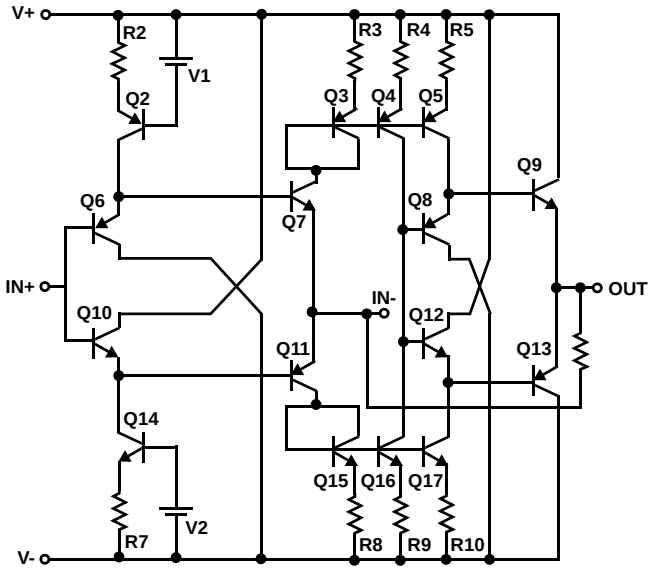


FIGURE 3. CURRENT FEEDBACK AMPLIFIER SIMPLIFIED SCHEMATIC

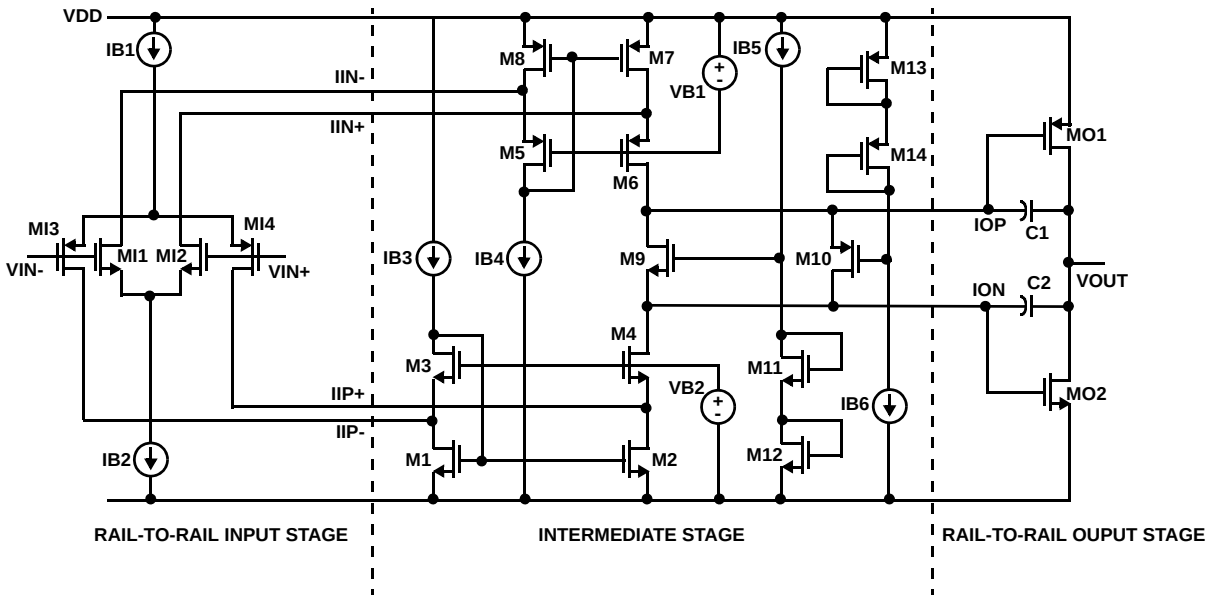
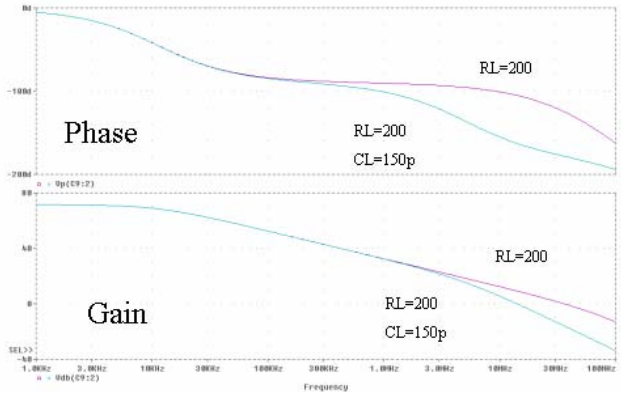


FIGURE 4. SIMPLIFIED SCHEMATIC OF A CMOS RAIL-TO-RAIL I/O AMPLIFIER

CMOS Rail-to-Rail Input/Output Amplifier

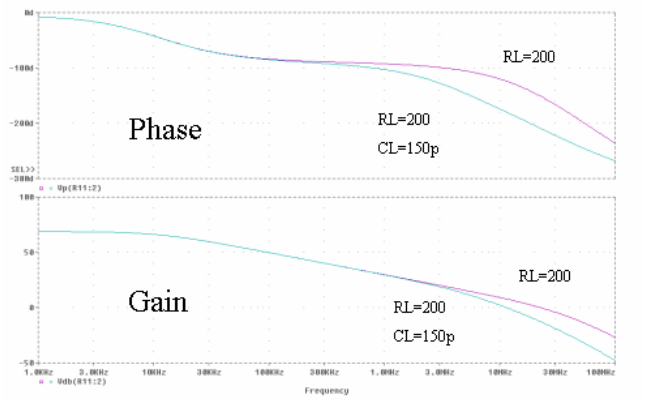
The simplified schematic of a CMOS rail-to-rail I/O amplifier, EL5411 is depicted in Figure 4. Consists of 3 stages - rail-to-rail input stage, intermediate gain stage and rail-to-rail output stage. The input stage is differential voltage input and differential current output. Its bandwidth extends to over 320MHz. The majority of the phase shift occurs over 100MHz beyond the bandwidth of the amplifier translating into generous phase margin The gate capacitance of the differential input stage MOS transistors and package lead capacitance combine for 2.5pF of amplifier input capacitance. Where as the dominant pole of this topology is set by internal compensation capacitors C_1 and C_2. This stage converts differential current into differential voltage at the output; so we have differential voltage input and single ended output. To simplify analysis, we assume the input stage is a differential voltage buffer with unity gain and the voltage gain of the gain stage is 50dB with the dominant pole occurring at 11kHz. The output stage is rail to rail topology utilizing transistors connected in common source configuration. Unlike source follower buffer output stages, the large gain of the common source output stage changes with the output-loading resistor while the bandwidth changes with the output loading resistor and load capacitance. The complete amplifier open loop frequency response shown above is a combination of input, gain and output frequency responses. The 150pF loading capacitance reduces the bandwidth of the output stage resulting in an overall system bandwidth decrease and phase margin reduction of 17°, a marginally stable condition. When in unity gain configuration the buffer configuration with Vout and Vin- directly shorted, the amplifier can drive 150pF and 200Ω load while remaining stable. The trouble occurs when resistor is placed in the feedback path.



R_{LOAD}	C_{LOAD}	GBWP	PHASE MARGIN
200Ω	NO	35MHz	56°
200Ω	150pF	14MHz	17°

FIGURE 5. CMOS RAIL TO RAIL AMPLIFIER OPEN LOOP RESPONSE

F is the feedback resistor, R_G is the gain resistor. If we select reasonable component values -- R_F = 3k and R_G = 8.3k. the feedback network combined with the 2.5pF capacitor at the negative input forms a low pass network from the amplifier output to the negative input. The frequency response of this feedback network shows -45° phase shift at 30MHz. The frequency response of the complete system including feedback network is shown in Figure 6. The feedback network reduces the overall system gain slightly because of the extra pole introduced by the feedback network. The most negative impact of this additional pole is that it reduces the phase by a significant amount. Under 150pF and 200Ω loading condition, the system with R_F = 3k, R_G = 8. 3k feedback network has 11.5MHz gain bandwidth product and 0° phase margin and the system oscillates.

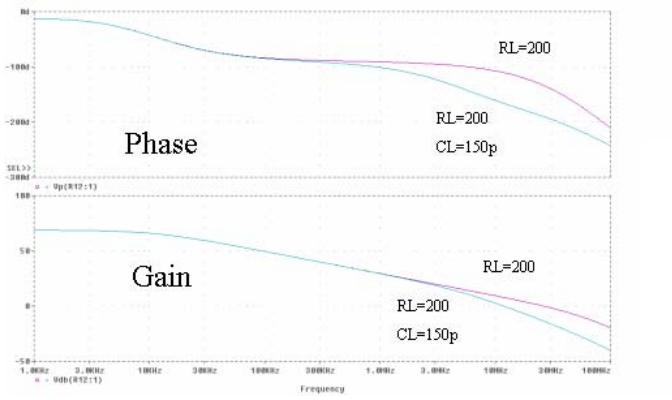


R_{LOAD}	C_{LOAD}	GBWP	PHASE MARGIN
200Ω	NO	22.5MHz	30°
200Ω	150pF	11.5MHz	0°

FIGURE 6. COMPLETE LOOP FREQUENCY RESPONSE WITH 3K R_F AND 8.3k R_G FEEDBACK NETWORK

Reduce feedback resistor value to minimize the impact of Cin

The phase shift and the loss of phase margin is caused by the action of the R_F-R_G-C_{IN} low pass filter. Reducing the R_F and R_G values will shift this low pass filter pole to a higher frequency (>30MHz). In the above example, as R_F and R_G values decrease 3X the pole moves from 30MHz to around 90MHz. Figure 7 shows the complete system frequency response with 3X smaller R_F and R_G values. This is a very nice solution because the gain bandwidth product changes very little while phase margin improves significantly. Under 200Ω and 150pF condition, the phase margin increases to 14° from 0°. The system is now stable. The minor trade-off with this solution is the amplifier now drives a 1k feedback, resulting in slightly increased power dissipation.

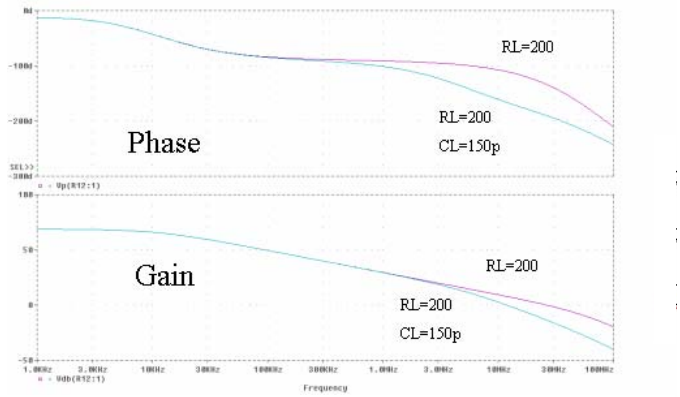


R_{LOAD}	C_{LOAD}	GBWP	PHASE MARGIN
200Ω	NO	25.7MHz	47°
200Ω	150pF	11.7MHz	14°

FIGURE 7. COMPLETE LOOP FREQUENCY RESPONSE WITH LOWER R_F AND R_G VALUES

Place Ccomp in parallel with R_F

This solution introduces a small compensation capacitor (Ccomp) in parallel with R_F without changing the values of R_F and R_G. The Ccomp capacitor introduces a phase lead to cancel out the phase lag caused by Cin. The complete system frequency response with 5pF Ccomp capacitor is shown in figure 8. The gain bandwidth product changes very little, however, the phase margin improves significantly. Under 200Ω and 150pF condition, the phase margin increases to 19° from 0°. The system is now stable with an additional Ccomp capacitor while maintain minimum power consumption.

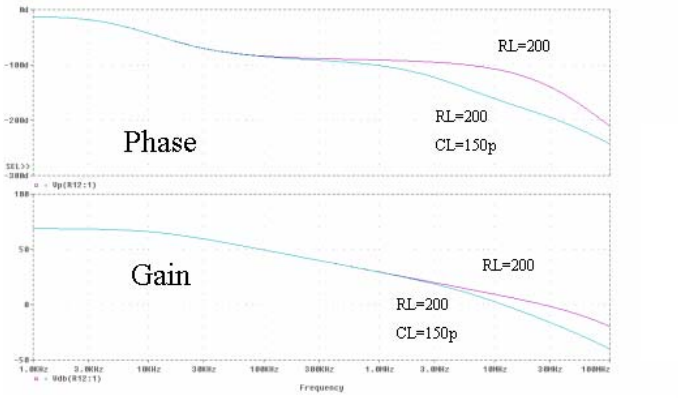


R_{LOAD}	C_{LOAD}	GBWP	PHASE MARGIN
200Ω	NO	25.7MHz	47°
200Ω	150pF	11.7MHz	14°

FIGURE 8. COMPLETE LOOP FREQUENCY RESPONSE WITH 5pF C_{COMP}

Increase close loop gain

The solution utilizes a large R_F and R_G ratio to increase closed loop gain. We use 43k R_F and 8.3k R_G in our example. The gain and phase curves of this R_F and R_G combination show a pole at 9MHz with -16dB attenuation. The -16dB attenuation reduces the overall system gain by 16dB. The complete system frequency response with large close loop gain is in Figure 9. The overall system open loop gain reduces by 16dB, decreasing to 54dB from 70dB. As a result, the gain bandwidth product decreases to around 5MHz. Therefore, the phase margin improves significantly. Under 200Ω and 150pF condition, the phase margin increases to 20° from 0°. The system is now stable by sacrificing bandwidth.



R_{LOAD}	C_{LOAD}	GBWP	PHASE MARGIN
200Ω	NO	25.7MHz	47°
200Ω	150pF	11.7MHz	14°

FIGURE 9. COMPLETE LOOP FREQUENCY RESPONSE WITH LARGE CLOSE LOOP GAIN

Unlike traditional amplifiers, the common source output stage of the rail-to-rail I/O amplifier has gain and bandwidth more sensitive to resistive a capacitive loading. The bandwidth variation along with the input capacitance significantly impacts amplifier stability. This application note has presented circuit designs of a rail-to-rail input and output CMOS amplifier where 3 possible solutions to the challenge of reducing amplifier instability have been discussed

1. Feedback resistor value reduction to minimize the impact of C_{IN}.
2. Introduction of a Ccomp in parallel with R_F.
3. An Increase of closed loop gain.

RLOAD (Ω)	CLOAD (pF)	GBWP (MHz)	PHASE MARGIN
200	No	6.7	52.3
200	150	4.5	20